CLAIMS

What is claimed is:

1. An interposer comprising:

a substrate comprising a B-stage adhesive material, and having an upper surface and a lower surface;

one or more first electrical contacts on the lower surface;

one or more second electrical contacts on the upper surface, the second electrical contacts having greater surface area, and greater pitch than the first electrical contacts; and

one or more first electrical pathways passing through the substrate, and connecting the first electrical contacts to the second electrical contacts.

2. The interposer as recited in claim 1 wherein the first and second electrical contacts are connection pads.

3. A substrate and semiconductor wafer assembly comprising:

a substrate comprising a B-stage adhesive material, and having an upper surface and a lower surface, one or more first electrical contacts on the lower surface, one or more second electrical contacts on the upper surface, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts, one or more first electrical pathways passing through the substrate, and connecting the first electrical contacts to the second electrical contacts;

a semiconductor wafer including one or more semiconductor dies, and having a first surface and a second surface, one or more third electrical contacts on the first surface of the semiconductor wafer, the third electrical contacts being associated with the semiconductor dies;

a conductor electrically connecting each first electrical contact with a corresponding third electrical contact; and

a layer of no-flow underfill disposed between the first surface of the semiconductor wafer and the lower surface of the substrate.

4. The substrate and semiconductor wafer assembly as recited in claim 3 wherein the first, second and third electrical contacts are connection pads.

5. The substrate and semiconductor wafer assembly as recited in claim 3 wherein each conductor is a solder ball.

6. The substrate and semiconductor wafer assembly as recited in claim 3 wherein each conductor comprises a conductive-polymer containing adhesive.

7. The substrate and semiconductor wafer assembly as recited in claim 3 wherein each conductor comprises a conductive plastic.

8. A method of producing a semiconductor wafer-interposer comprising the steps of:

attaching one or more first electrical contacts to a lower surface of a substrate comprising a B-Stage adhesive material;

attaching one or more second electrical contacts to an upper surface of the substrate, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts; and

creating one or more first electrical pathways passing through the substrate and connecting the first electrical contacts to the second electrical contacts.

9. The method as recited in claim 8, wherein the first and second electrical contacts are connection pads.

10. A method for producing a wafer-interposer assembly comprising the steps of:

attaching one or more first electrical contacts to a lower surface of a substrate, the substrate comprising a B-Stage adhesive material;

attaching one or more second electrical contacts to an upper surface of the substrate, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts;

creating one or more first electrical pathways passing through the substrate and connecting the first electrical contacts to the second electrical contacts;

depositing a conductor on one or more third electrical contacts on an upper surface of a semiconductor wafer, the semiconductor wafer including one or more semiconductor dies and the third electrical contacts being associated with the semiconductor dies;

applying a layer of no-flow underfill to the upper surface of the semiconductor wafer;

aligning the substrate with the semiconductor wafer so that the deposits of the conductor on the third electrical contacts correspond with the first electrical contacts on the lower surface of the substrate;

attaching the substrate to the semiconductor wafer.

11. The method as recited in claim 10 wherein the first, second and third electrical contacts are connection pads.

12. The method as recited in claim 10 further comprising the step of curing the B-Stage adhesive, the conductors, and the underfill.

13. The method as recited in claim 10 further comprising the step of applying additional metalization to one or more of the third electrical contacts to redistribute them prior to the attachment of the substrate.

14. The method as recited in claim 10 further comprising the step of adding additional metalization to one or more of the third electrical contacts to improve the contact between the conductor and the third electrical contacts.

15. The method as recited in claim 10 where in the step of attaching the substrate to the semiconductor wafer comprises the steps of:

placing the semiconductor wafer on a first flat surface and holding the semiconductor wafer in place;

coating a second flat surface with a material that will prevent adhesion of the substrate;

placing the substrate on the second flat surface and holding the substrate in place; and

bringing the first and second flat surfaces together so that the semiconductor wafer and the substrate form an adhesive bond.

16. The method as recited in claim 10 further comprising the step of singulating the substrate and semiconductor wafer assembly into one or more semiconductor die assemblies.

17. The method as recited in claim 10 wherein the cured B-Stage adhesive forms a rigid bond.

18. The method as recited in claim 10 wherein the cured B-stage adhesive forms a semi-rigid bond.

19. The method as recited in claim 10 wherein the cured B-Stage adhesive forms a compliant bond.

20. The method as recited in claim 10 wherein each conductor is a solder ball.

21. The method as recited in claim 10 wherein each conductor comprises a conductive-polymer adhesive.

22. The method as recited in claim 10 wherein each conductor comprises a conductive plastic.

23. The method as recited in claim 10 further comprising the steps:

attaching the substrate and semiconductor wafer assembly to a testing apparatus; and

testing at least one of the semiconductor dies.

24. The method as recited in claim 23 wherein the step of testing the semiconductor dies further comprises performing parametric testing on at least one of the dies.

25. The method as recited in claim 23 wherein the step of testing the semiconductor dies further comprises performing burn-in testing on at least one of the dies.

26. The method as recited in claim 23 wherein the step of testing the semiconductor dies further comprises testing the semiconductor dies in sequence.

27. The method as recited in claim 23 wherein the step of testing the semiconductor dies further comprises testing the semiconductor dies simultaneously.

28. The method as recited in claim 23 further comprising the step of grading one or more performance characteristics of each semiconductor die during testing.

29. The method as recited in claim 28 further comprising the step of singulating the substrate and semiconductor wafer assembly into one or more semiconductor die assemblies.

30. The method as recited in claim 29 further comprising the step of sorting the semiconductor die assemblies based on the one or more performance characteristics.

31. The method as recited in claim 29 further comprising the step of sorting the semiconductor die assemblies into conforming and nonconforming groups.